# Fundamental Energy Efficiency Measures for Home Gateways

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## ABSTRACT

This poster describes the specification and development of an integrated solution for energy efficient home gateways. The effect of energy efficiency measures is demonstrated by results from a reference product implementation.

In the first part an introduction to the home gateway and the main energy saving challenge is given. The home gateway forms the entry point for broadband internet services and is the central in-house communication device. It has to provide always available services and "always on" functionality. As reference today's standard usage times are shown as diagram. Values are 1.9 hours "ON", 18.2 hours "Low Power" and 3.4 hours "OFF" and 0.5 hours "Zero Watt OFF". These values are based on usage time studies [1] of home gateway internet devices. In the original study the "Low Power" category is named as "standby" but from considering definitions in [2, 3, 4] it becomes clear that "Low Power State" is meant here rather than "standby". As final part of the introduction the solution approach for highly energy efficient products by in depth use-case analysis is highlighted. As example the minimum active functions for the "Low Power State" as specified by the European Code of Conduct on Energy Consumption of Broadband Equipment [4] are given:

- A DSL IP connection is required to receive VoIP calls. For transmission of IP stream the physical layer must be kept active which means that DSL tones are permanently active and analyzed in the system.
- WLAN base station function must be capable of performing association of new mobile devices to the WLAN network and maintain the wireless link to previously associated devices. For this the WLAN has to transmit beacon and to operate the receive path. In general Wi-Fi standards must be fulfilled.
- Ethernet link detection must be active and attached devices must be managed when requesting new link and 802.3 standards must be fulfilled.
- For DECT / CatIQ cordless telephony interface incoming call detection must be assured. Therefore DECT/ Cat IQ scanning are active or beacon is send. Ringing must be delivered. This is required for all telephony interfaces.
- The telephone interface FXS has to detect off-hook. Attached telephones must be fed.
- Incoming calls at the FXO telephone interface must be detected.
- Attachment of new devices to USB must be recognized


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As key element of energy efficient solution the system architecture is specified on basis of use case analysis to keep the hardware components active at lowest possible level always. For this the energy efficiency aspect must be evaluated and implemented on all levels of design process.

In the following sections different key aspects required for developing energy efficient system architecture are discussed namely: The power supply system, interface system architecture, processor memory system, hardware measures and software and firmware.

The power supply system composed of the external power adapter and on-board DC-DC conversion has an important impact on the overall system energy consumption. This is shown for the example of a typical IAD On-state power consumption using a non optimized power supply. Here up to 65% of the system power is lost in the power supply. Optimizing DC-DC converters and external power supply is shown to save in the order of 40% system power.

Interface system architecture is of highest importance to keep system power low. Interfaces should support enhanced low power mechanisms as explained below:

- xDSL : Full support of L2 and L3 power saving Modes
- Ethernet : Energy Efficient Ethernet [5], Low Power Link Detection,
- WLAN: Noise dependent TX Power adaption, Interrupt free Beacon Only Mode
- DECT / CatIQ: Low Power NEMO Mode, Interrupt free Beacon Only Mode
- FXS Telephony: Low Power Standby Mode, Automated High Voltage Reduction, Automatic Phone Plug Detection
- USB: Full Suspend and Resume support

The scheme of the developed Energy Efficient Ethernet [5] implementation with LPI state is explained in a diagram.

Energy efficiency of central processor memory system can be improved by maximizing the instruction per cycle (IPC) figure. The tremendous increase in processor speed in comparison to (off-chip) memory speed has led to the "memory wall" problem [6, 7]. As consequence the processing performance cannot be effectively used leading to "stall" cycles wasting energy. Measures like cache size dimensioning, multi way caches, tightly coupled memories and hardware multi threading are to be considered. Measurements results for hardware multithreading performance boost for a product using 34K MIPS architecture is shown together with the principle diagram of saving energy by reduced "stall" cycles.

Following hardware measures have to be considered when creating a new device.

- Low Power Technology Selection
- Automated local Hardware Clock Gating
- Peripheral Level Clock Gating
- Global Clock Gating
- Processor Instruction based Clock Gating
- Dynamic Voltage scaling
- Power Islands

Usefulness of some hardware measures is technology dependent while all clock gating related measures are mandatory.

Software, Operating system and Firmware are fundamental in using the hardware features efficiently. Firmware has to support the implementation of low level saving protocols. Power management software is taking care of adaption of hardware states to the application performance requirements. Power saving functions like DRAM power down must be enabled in time.

The operating system must offer support for software power management for example WAIT instruction. Abstraction of hardware functionality with system states similar to ACPI [8] is required to decouple higher level power management from hardware details. Finally a power management API is making power saving functions available to application software.

In conclusion the effect of energy efficiency measures is demonstrated by comparing power measurement results from a typical non optimized 3rd party product and the energy optimized reference solution. Power targets as defined by European Code of Conduct [4] are also shown in the diagram for comparison.

Further improvements in energy efficiency may be obtained by

- Integration of "Always On" products to Home Gateway thereby improving overall system power
- Enabling attached products to enter lower power states
- Further architectural optimization for devices with higher functionality
- Intelligent control of household devices
- E - Metering

## Categories and Subject Descriptors

C.2.0 [**Computer-Communication Networks**]: General – *Data communications.* Additional category and subject descriptors: J.7 [**Computers in other systems**]: Consumer Products –

## General Terms

Design, Measurement, Performance, Standardization.


## Keywords

Home Gateway, DSL, Energy Efficiency, Use case, Code of Conduct, Processor System, Energy Efficient Ethernet.


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