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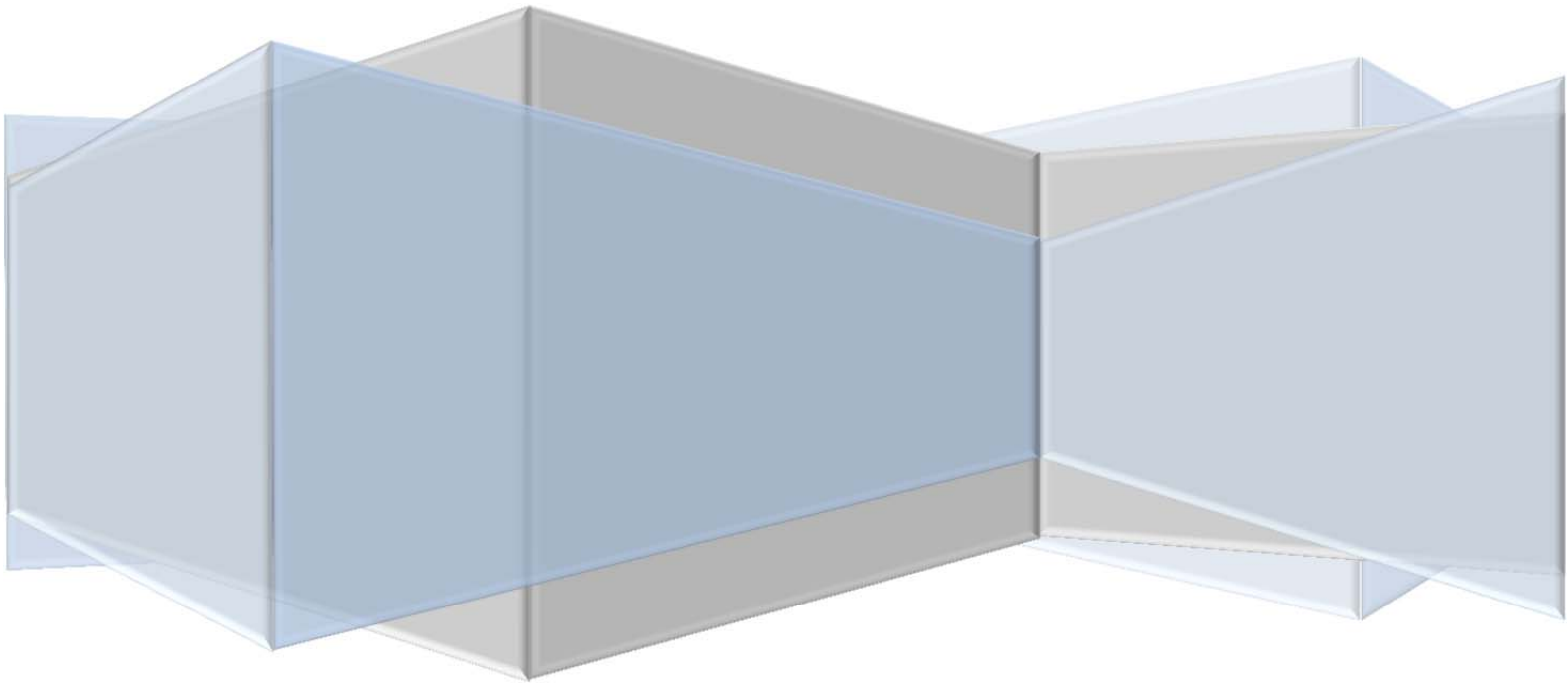

Session 1: BIST and ATPG

Built-in Test in Wireless Systems Using Non-Intrusive Sensors

by Athanasios DIMAKOS, TIMA Laboratory (CNRS – Grenoble INP – UJF), France

Advisors: Haralampos-G. STRATIGOPOULOS, Salvador MIR

Current and new-generation electronic systems and devices (e.g. automotive electronics, portable and hand-held devices, computers, sensor networks, and biomedical implant devices) increasingly rely on wireless communication. As the performance expectations for wireless communication systems grow (e.g. stringent specifications, dense integration with other heterogeneous components, higher speed, lower power consumption, networking flexibility), their testing becomes more challenging and complex. In fact, it is reported that testing the RF parts of a wireless system can amount up to half of the overall manufacturing cost.

In this work, we develop built-in test solutions for RF circuits, in order to circumvent the need for elaborate test instrumentation and reduce the cost of RF test. The underlying idea is to build on-chip some auxiliary circuitry that extracts useful information about the circuit under test (CUT). The key characteristic of the proposed built-in test solutions is that they are non-intrusive, that is, they are transparent to the CUT and do not degrade its performances. Recently it was proposed to test RF circuits non-intrusively by employing variation-aware sensors. These sensors are basic analog stages that mimic part of the CUT architecture (we refer to them as dummy circuits) and process-control monitors (PCMs). They are placed in close proximity to the CUT on the same substrate without being electrically connected to it. Instead, their operation is based on the fact that they undergo the same process variations as the CUT. As a result, any degradation in the CUT's performances is reflected in the sensor outputs, which shift away from their nominal values. In essence, we capitalize on an undesired phenomenon – inter-die process variations – to minimize the cost of the RF test. In this work, we enhance the library of non-intrusive sensors. In particular we study how ring oscillators can be employed to track variations in the performances of an RF LNA.

Accurate QBF-based Test Pattern Generation in Presence of Unknown Values and beyond

*by **Dominik Erb**, Stefan Hillebrecht, Michael Kochte, Hans-Joachim Wunderlich, Bernd Becker;*
Albert-Ludwigs-University, Freiburg, Germany

Unknown (X) values may emerge during the design process as well as during system operation and test application. Sources of X-values are for example black boxes, clockdomain boundaries, analog-to-digital converters, or uncontrolled or uninitialized sequential elements.

To compute a detecting pattern for a given stuck-at fault, well defined logic values are required both for fault activation s well as for fault effect propagation to observing outputs. In presence of X-values, classical test generation algorithms, based on topological algorithms or formal Boolean satisfiability (SAT) or BDD-based reasoning, may fail to generate testing patterns or to prove faults untestable.

This work proposes the first efficient stuck-at fault ATPG algorithm able to prove testability or untestability of faults in presence of X-values. It overcomes the principal inaccuracy and pessimism of classical algorithms when X-values are considered. This accuracy is achieved by mapping the test generation problem to an instance of quantified Boolean formula (QBF) satisfiability. For sequential circuits an additional expansion is proposed which observes several time frames.

The resulting improvement of fault coverage is shown on experimental results based on ISCAS benchmark and larger industrial circuits.

Provably Optimal Test Cube Generation Using Quantified Boolean Formula Solving

*by **Sven Reimer**, Matthias Sauer, Ilia Polian, Tobias Schubert, Bernd Becker*
Albert-Ludwigs-University, Freiburg, Germany

Circuits that employ test pattern compression rely on test cubes to achieve high compression ratios.

The less inputs of a test pattern are specified, the better it can be compacted and hence the lower the test application time. Although there exist previous approaches to generate such test cubes, none of them are optimal.

We present for the first time a framework that yields provable optimal test cubes by using the theory of quantified Boolean formulas (QBF). Extensive comparisons with previous methods demonstrate the quality gain of the proposed method.

A Scan-Out Power Reduction Method for Logic BIST

by Senling Wang, Kyushu Institute of Technology, Japan

Excessive power dissipation in logic BIST can cause several problems such as yield loss or circuit destruction. Although many low power BIST approaches that reduce power dissipation at scan-shift operation have been proposed, they only focus on controlling the scan-in power by modifying test patterns with low switching activity, and the scan-out power that determined by test responses is out of considering. For controlling the total scan-shift power, scan-out power control remains as an important issue. In our research, we propose a novel approach that focuses on reducing the scan-out power as well as scan-in power reduction for logic BIST. The proposed approach overwrites some flip-flop values before starting scan-shift so as to reduce the switching activity at scan-out operation. Experimental results show that the proposed approach reduces scan-out power up to 50% with little fault coverage loss and little hardware overhead.

Session 2: Complex Systems Engineering

Achieving Fairest Distribution of Resources Collectively: Complexity and Algorithms

by Wenjing Rao, University of Illinois, Chicago, USA

We focus on the problem of decentralized resource allocation in a locally connected network. Bounded by the network constraint, each resource can only be allocated to one of the local agents. However, a global ``fairest distribution" has to be achieved despite the connectivity constraint. It seems that not only does a fairest distribution exists, such a global optimum can be approached via ``local balancing" based steps as well. Based on such observations, we propose some decentralized protocols that can efficiently converge to a near-optimal solution by taking advantage of concurrent resource transfers via localized communication only.

Ants in NoC

by Rüdiger Ibers, University of Paderborn, Germany

In modern System-on-Chip designs the number of IP cores is continuously growing. For these designs, a network-on-chip (NoC) seems to be a good interconnect architecture. But an efficient and reliable communication between the cores depends mainly on the used routing protocol.

In this talk, a new high level network on chip simulator is introduced to evaluate and visualize the efficiency of different routing algorithms. This simulator was designed with respect to an already existing NoC implementation described in VHDL. As an example, an ant colony optimization (ACO) algorithm is used to find the best path for the data packets traveling through the network. The low memory overhead and the adaptive nature of this algorithm are visualized.

Ensuring Reliability of 3D-ICs

by Carolina Metzler, LIRMM, Montpellier, France

Three-Dimensional (3D) Integrated Circuits (IC) is an emerging technology that promises to solve the interconnect bottleneck problem by vertically connecting tiers with Through Silicon Vias (TSVs). TSVs provide shorter and faster interconnects than the conventional 2D interconnects due to reduced lengths and parasitics enabling signal transmission, power and clock lines among multi-stacked tiers. Despite the on-going advancements on 3D processing technologies, 3D test is still immature. The multitude of manufacturing steps can introduce a lot of undesirable effects that can alter TSV performance or even lead to TSV failure.

The objective of this PhD thesis is to investigate reliability issues in 3D ICs and develop 3D-aware test solutions by in-depth analyses of 3D failure mechanisms departing from TSV physical characterization and simulation. In this talk, we will present a TSV resistive open defect characterization. The analyses consider different physical and electrical conditions that tiers can experience i.e. power supply noise (voltage drop and ground bounce). We also consider TSV-to-TSV coupling (inductive and capacitive coupling), and different frequency range. Based on these analyses, we provide guidelines to improve TSV-aware test solutions, such as detection methods for resistive-open TSVs.

Towards Self-healing Integrated Circuits: Application of BIST for Auto-Adaptive RF Power Amplifiers

by Martin Andraud, TIMA Laboratory (CNRS - Grenoble INP - UJF), France

Advisors: Emmanuel Simeu, Haralampos-G. Stratigopoulos

Demands on the performances of wireless transceivers are constantly increasing to meet objectives such as ubiquitous connectivity and mass data transfer with high rates. In addition, in mobile applications wireless transceivers have to save a maximum of energy to contribute to battery life extension. Those stringent requirements must be met in modern CMOS technologies (e.g. 65nm and below) and take into account the exacerbated process variations which can lead to dramatic yield loss.

Moreover, during its lifetime the wireless transceiver operates under variable channel conditions. On one hand, favorable conditions may lead to wasted energy whereas harsh conditions may result in communication errors unless real-time power adaptation is used. On the other hand, ageing effects may lead performances to be degraded. All those elements are undesirable, especially for remote, safety-critical, and mission-critical systems.

In this context, this work aims at designing a self-healing RF power amplifier which checks and adapts its performances, in order to continuously operate at optimal power while satisfying the performance requirements. The self-healing mechanism will be used for a first auto-calibration to compensate for manufacturing process variations and on-line adaptation during the lifetime of the circuit to adapt its power consumption and to tolerate ageing effects. To achieve the self-healing property, the circuit will include (a) BIST functions to extract information-rich signatures, (b) tuning knobs that add freedom in the design and ideally act orthogonally on the performances, and (c) a feed-back loop that translates the test signatures into

Session 3: Complex Systems Engineering

Signal Integrity- Aware Pattern Generation for Delay Testing

by Anu Asokan, LIRMM, Montpellier, France

Deep submicron impacts are nowadays more prominent in Nanoscale devices due to high speed switching and the defects in manufacturing process. These are the major reasons for low-circuit performance (such as delay variation, functionality error etc.) and Defective parts per million (DPPM). Existing delay testing techniques do not capture the impact of combined effects of power supply noise, crosstalk and ground bounce for critical path delay analysis. They capture the worst case power supply noise in order to obtain the worst case path delay. We show that such assumption is not necessarily sufficient and combined effects of Crosstalk, Power and Ground noise should be considered for path delay analysis. First, we propose accurate close-form mathematical models for capturing the path delay variations in the presence of power supply noise and ground bounce. We utilize these models as the fitness function for pattern generation technique which is a simulated annealing based iterative process. In our experiments, we show that path delay variation can be significant if test patterns are not properly selected.

Controllability Analysis of Local Switching Activity for Layout Design

*by **Kohei Miyase**, Matthias Sauer, Bernd Becker, Xiaoqing Wen, Seiji Kajihara,*
Albert-Ludwigs-University, Freiburg, Germany

Recently, ATPG and X-filling utilize layout information in order to achieve desired results. Especially, low-power ATPG have to reduce the power in a part of circuit where the many switching activities occur. In this work, we analyze the controllability of switching activity in a specific part of circuit. For ITC'99 benchmark circuit, we visualize the analyzed results. Finally, we discuss how to use them in ATPG and X-filling.

A Mixed Mode Simulation of Delay Induced by IR-Drop

by Jie Jiang, University of Passau, Germany

As today's deep submicron technology scales down, power supply noise is more concerned than ever since designs are becoming more sensitive to power supply noise due to reduced supply voltage and increased power density. Both two major kinds of power supply noise, the inductive voltage noise (L.di/dt) and the resistive voltage noise (IR), can increase the gate propagation delay, which in turn degrades the circuit performance and even leads to functional failure. Our research focuses on the IR-drop effect. We propose a mixed mode simulation of IR-drop induced delays , which performs a vector-based simulation at logic level while a realistic resistive model of the Power Distribution Network (PDN) is integrated in the model, and the IR-drop effect is taken into account based on the pre-characterization of the library. The purpose is to simulate the IR-drop effect as accurately as possible in compromise to the timing performance of the simulator.

Multi-Stage Fault Attacks on Block Ciphers

by Philipp Jovanovic, University of Passau, Germany

An algorithm is presented to cryptanalyse block ciphers with independent subkeys using differential fault analysis [1]. In the second part we execute the algorithm on a concrete example: The new low-cost block cipher PRINCE [2] serves as a target and we show how to reconstruct it's 128-bit key k requiring only a few fault injections. First correct / faulty ciphertext pairs (c_i, c'_i) are generated. After that mathematical analysis is used to exploit the strong relations between c_i and c'_i to quickly eliminate wrong candidates for k. Experiments show that the number of remaining key candidates is practical for performing a brute-force search.

[1] https://en.wikipedia.org/wiki/Differential_fault_analysis

[2] http://eprint.iacr.org/2012/529

Session 4: Fault Tolerance

Identification of Critical Variables using an FPGA-based Fault Injection Framework

*by **Andreas Riefert**, Jörg Müller, Matthias Sauer, Wolfram Burgard, Bernd Becker,*
Albert-Ludwigs-University, Freiburg, Germany

The shrinking nanometer technologies of modern microprocessors and the aggressive supply voltage down-scaling drastically increase the risk of soft errors. In order to cope with this risk efficiently, selective hardware and software protection schemes are applied. In this paper, we propose an FPGA-based fault injection framework which is able to identify the most critical registers of an entire microprocessor. Furthermore, our framework identifies critical variables in the source code of an arbitrary application running in its native environment. We verify the feasibility and relevance of our approach by implementing a lightweight and efficient error correction mechanism protecting only the most critical parts of the system. Experimental results with state estimation applications demonstrate a significantly reduced number of critical calculation errors caused by faults injected into the processor.

Efficient Observation Point Selection for Hardware Aging Monitoring

by Chang Liu, University of Stuttgart, Germany

Technology scaling threatens circuit reliability. One of the concerns is the susceptibility to transistors aging. Using stability checkers (SC) to detect the accumulating delay increase along the critical or long paths is one well-known and commonly utilized approach. However, during functional operation, it is possible that some long paths with aging checkers are not sensitized very often, and may lead to unmonitored aging progress. To avoid this situation, we propose a novel stability checker placement/relocation method. Instead of integrating the aging sensors only in flip-flops (FF) at the end of the critical or long paths, the stability checkers are inserted at the meticulously selected observation points (OPs). The experimental results prove the efficiency of the proposed methodology.

Towards Fault Tolerant LTE-MIMO detectors

by Victor Tomashevich, University of Passau, Germany

Nanoscale effects due to transistor shrinking cause transient faults or soft errors at upper layers of contemporary hardware. The impact of soft errors on the performance of specific signal processing hardware is becoming of interest in recent years due to further technology downscaling. Current approaches concentrate either on small subcircuits and make design assumptions, which do not always conform with real implementation. In that case it is often not feasible to draw conclusions on the severity of impact of soft errors on system performance. The effect of errors in system memories of Sphere Detector implementation is analysed. The sphere detector represents a very complex ASIC which is capable of processing 4x4 MIMO communication links. The advantage of having a complete implementation is that it is possible to access the impact of soft errors on the performance of a complete receiver system.

Robustness Checking with ATPG

by Viktor Froese, University of Paderborn, Germany

Strongly fault secure networks achieve the totally self-checking (TSC) goal by guaranteeing that every error can either be detected or does not affect the circuit outputs even in the case of fault accumulation.

To verify this property, many possible fault sequences need to be considered. A speedup in multiple fault analysis can be achieved by reusing detectability or redundancy information of single faults for accumulated faults and by using the advances in incremental SAT-based ATPG.

But with the increasing parameter variability in nanoscale circuits traditional design methods for fault tolerant circuits are no longer sufficient. The second part of the talk gives an outlook on the challenges of robustness checking in the presence of parameter variations.

Session 5: Analog Mixed Signal and Delay Test

Phase Noise Measurement of Sinusoid Based Signal on Digital Test Equipment for Low-Cost Testing of Analog/RF Circuits

by Stéphane David-Grignot, LIRMM, Montpellier, France

The general context of this project is the development of low-cost methods to test Analog/RF devices. More specifically, the purpose is to develop solutions to perform analog measurements using cheap hardware resources. The idea is to use 1-bit level-crossing in order to convert an analog/RF signal into a digital bit stream. This conversion may be achieved by a simple comparator stage, that can be located on-chip or by using simple digital channel of standard test equipment. During this conversion, the information carried by the analog/RF signal (amplitude, frequency, phase…) is transformed into a timing information in the digital bit stream.

Amplitude measurement and frequency measurement algorithms have already been developed using such techniques on a sinusoid. The work carried out here is to develop a method to extract the phase noise of a sinusoid out of the digital bit stream. Modeling phase noise has been carefully studied and frequencies measured with this method have been found to be strongly bounded to the phase noise of the signal. It is possible to measure the phase noise even with low sampling frequencies. However the conditions under which this technique is reliable have still to be determined. A stochastic model and a study of the robustness of the process are being developed to address this issue.

PhD supervisors: Laurent Latorre, Florence Azais (LIRMM)

Employer: François Lefevre (NXP Semiconductors, Caen)

Development of technical test for analog integrated circuits

by Syhem Larguech, LIRMM, Montpellier, France

The general purpose of my research studies consists on the development of analog integrated circuits test method. We will focus on the indirect test method which consists on finding correlations between a set of low-cost measurements and a set of device performances. The idea is then to use correlation techniques to estimate the dynamic parameters from the measured ones. The challenge of such an indirect test technique is to find non-specified parameters (bias voltages, DC or low frequency parameters) that have a correlation with dynamic performances. Moreover, the validation of the correlation between indirect test parameters and dynamic performances is not an easy task because based on statistical data. This kind of test is recognized by this low-cost test and it becomes a promising research field. Such correlation is built with learning programs such as the Multivariate Adaptive Regression Spline (MARS).

Supervision: Serge Bernard, Florence

High-performance Time-Simulation of CMOS-Circuits

by Eric Schneider, University of Stuttgart, Germany

Time simulation of circuits has many uses in EDA and test.

While most classical approaches are optimized for fast evaluation at gate-level, they lack the precision that is needed to investigate first order effects introduced by the latest nanometer manufacturing processes.

Approaches based on SPICE models on the other hand, offer the required precision, but become infeasible for large designs due to complexity issues.

In this work, a method is presented that allows to efficiently simulate circuits at transistor-level on data-parallel architectures by offering a trade-off in simulation speed and precision enabling a wide field of applications.

Efficient SAT-Based Dynamic Compaction and Relaxation for Longest Sensitizable Paths

*by **Matthias Sauer**, Sven Reimer, Tobias Schubert, Ilia Polian, Bernd Becker,*
Albert-Ludwigs-University, Freiburg, Germany

Comprehensive coverage of small-delay faults under massive process variations is achieved when multiple paths through the fault locations are sensitized by the test pair set. Using one test pair per path may lead to impractical test set sizes and test application times due to the large number of near-critical paths in state-of-the-art circuits.

We present a novel SAT-based dynamic test-pattern compaction and relaxation method for sensitized paths in sequential and combinational circuits. The method identifies necessary assignments for path sensitization and encodes them as a SAT-instance. An efficient implementation of a bitonic sorting network is used to find test patterns maximizing the number of simultaneously sensitized paths. The compaction is combined with an efficient lifting-based relaxation technique. An innovative implication-based path-conflict analysis is used for a fast identification of conflicting paths.

Session 6: Debug and Diagnosis

Software-based Diagnosis

by Dominik Ull , University of Stuttgart, Germany

For over 30 years, software-based self-test (SBST) is a preferred, well-known, at-speed test method for processors that requires neither external nor integrated test hardware and can be applied in very flexible ways. Traditional debug and diagnosis, however, is based on additional on-chip scan infrastructure, automatic test equipment and in-system test access.

In this work, we propose a structural, software-based diagnosis method, bringing the advantages of software-based testing to the diagnosis domain. By transforming sequential processor pipeline structures into equivalent combinational replacements, combinational ATPG for test pattern generation and the location-based POINTER algorithm for structural diagnosis can be applied.

Adaptive Diagnosis for Intermittent Faults

by Thomas Indlekofer, University of Paderborn, Germany

The decreasing feature size of nanoelectronic circuits leads to new fault effects and new challenges in test and diagnosis: transient and intermittent faults can occur due to a higher susceptibility to external noises and dynamic parameter variations. While transient faults can be compensated during system operation by robust and self- adaptive designs, intermittent faults can be weak points in the design and occur in irregular intervals. Because of the similar behavior, a standard test cannot distinguish between non-critical transient and critical intermittent or permanent faults. On the one hand, this lead to quality problems if the test is too optimistic, on the other hand unnecessary yield loss due to a non-critical transient fault can occur.

Because of these problems, a diagnostic test procedure will be presented, which combines a window-based diagnosis with Bayesian reasoning to distinguish between permanent, transient and intermittent faults. The test is partitioned into shorter sessions and repeats only the sessions in which an error occurs. A diagnosis procedure calculates possible fault locations, while with the help of a Bayesian network the classification into the different types can be done adaptively during test. After presenting the procedure and the scheme, experimental results will be shown to validate this idea.

A New Method for Control Flow Error Detection Using Debug Interface

*by **Boyang Du**, M. Sonza Reorda, L. Sterpone, Politecnico di Torino, Italy*

We propose a new method for control flow-related error detection by taking advantage of the existing debug interface of the target processor. Many techniques have been proposed for control flow error detection and protection focusing on software, hardware or hybrid solutions. This new approach requires no modification of the software and no compiler support, so it overcomes the performance overhead caused by extra instructions used in software solutions; and it does not require any modification of the target processor, instead, it exploits the debug interface which is common on popular processors in the market, while accessibility of low level structure is not always available. To verify the effectiveness of the new method, we run experiments using the miniMIPS processor from OpenCores by adding a debug interface, and then use ModelSIM simulator to simulate the fault injection performed on the processor and a software environment to analyze and classify the faults we injected. Preliminary experimental results have been very promising for this new solution we propose.

Session 7: FPGA and Memory Test

Development of Test Time Reduction Methodology for a Novel SRAM & Cluster-based FPGA

by Saif-Ur Rehman, TIMA Laboratory, Grenoble, France

The tremendous development of CMOS technology has enabled an increasing integration density according to Moore's Law. However, this trend of evolution is being slowed due to economic and physical limits. As yield goes down, one of the key challenges of the coming years is to find a way to use a maximum of fabricated circuits while tolerating physical defects spread all over the chip. To this end, in the framework of a French National Research Project (ANR) called Robust FPGA, a design of a defect tolerant FPGA is under development.

To achieve the fault tolerance goal, synthesis/configuration tools are developed to enable the bypass of defective blocks and to enable implementation of applications on the defect free blocks.

One of the objectives of the project is to propose a methodology to efficiently test the new cluster-based FPGA architecture. Processing the test results will allow the generation of a map of defective blocks, this map being a required input to implement fault avoidance techniques.

In this context, a first test solution explored consists in taking advantage of the functional resources of the FPGA through the use of a BIST mechanism. As the time for FPGA configuration dominates the overall test time, the main challenge consists in reducing the required number of test configurations as well as improving the configuration bit-stream loading mechanism. This presentation focuses on the efficient usage of the novel FPGA resources for the logic blocks test time reduction. The cluster-based architecture of the FPGA facilitates the implementation of this BIST technique, offering high fault coverage with almost no additional hardware.

Magnetic Memory Testing from MRAM to MLU

by João Azevedo, LIRMM, Montpellier, France

Since the Giant Magneto-Resistance (GMR) effect discovery by P. Grünberg and A. Fert a special attention has been given to one of the most interesting and challenging branch in today's nanotechnology called "Spintronics". This technology prompted scientific research and microelectronic industry to think about alternatives to replace especially non-volatile memories. Thermally Assisted Magnetic RAMs (TAS-MRAMs) are "Spintronics" devices that offer several advantages when compared to FLASH and SRAM memories. In addition to TAS-MRAMs, a new concept of Self-Reference TAS cell (SR-TAS) is being developed and can be used as a true logic element called Magnetic Logic Unit (MLU). In order to provide effective test solutions for these "Spintronics" devices it is mandatory to understand how they work.